CY7C1018CV33

128K x 8 Static RAM

Features

- **Pin- and function-compatible with CY7C1018BV33**
- **High speed**
  - **t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Data retention at 2.0V**
- **Automatic power-down when deselected**
- **Easy memory expansion with CE and OE options**
- **Available in Pb-free and non Pb-free 300-mil-wide 32-pin SOJ**

Functional Description[1]

The CY7C1018CV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

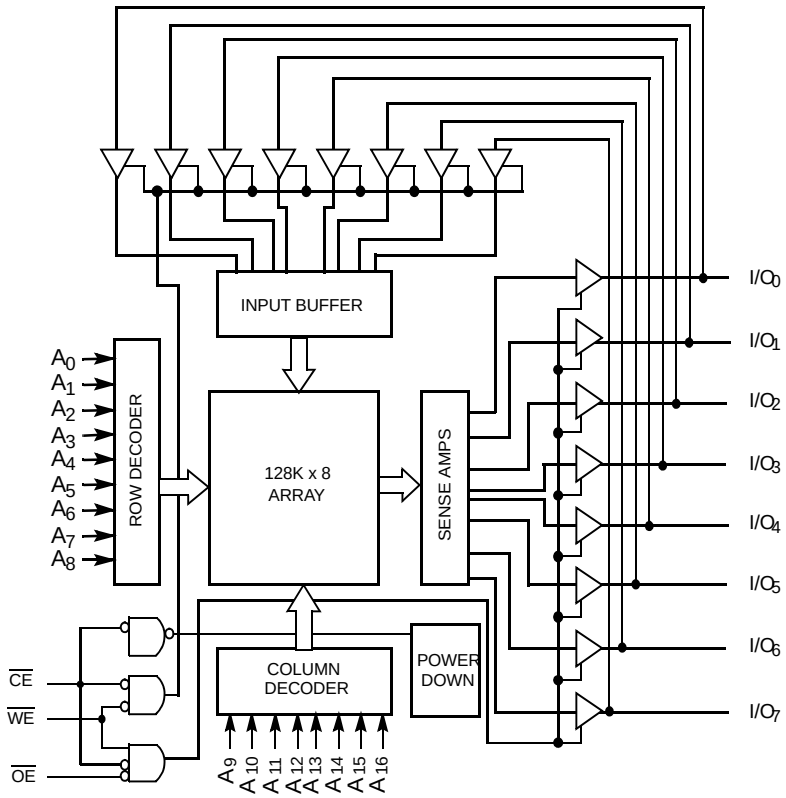
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

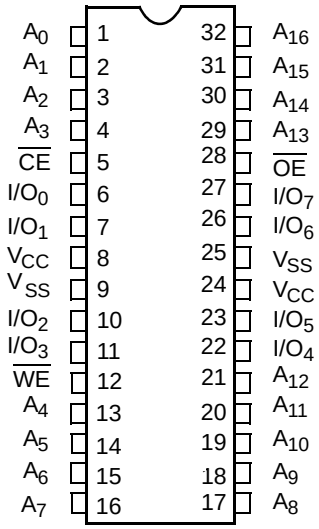
The CY7C1018CV33 is available in a standard 300-mil-wide SOJ.

Logic Block Diagram



Pin Configurations

SOJ
Top View



Note:
1. For guidelines on SRAM system designs, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Selection Guide

		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Comm'l	90	85	80	mA
	Ind'l		85		mA
Maximum Standby Current		5	5	5	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[2] ... –0.5V to + 4.6V

DC Voltage Applied to Outputs[6] in High-Z State .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		–10 Min.	–10 Max.	–12 Min.	–12 Max.	–15 Min.	–15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Comm'l		90		85		80	mA
			Ind'l				85			mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Comm'l		15		15		15	mA
			Ind'l				15			mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Comm'l		5		5		5	mA
			Ind'l				5			mA

Capacitance[3]

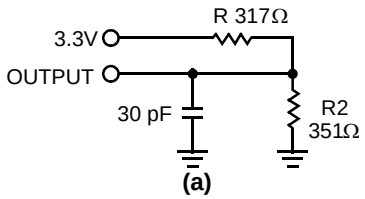
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

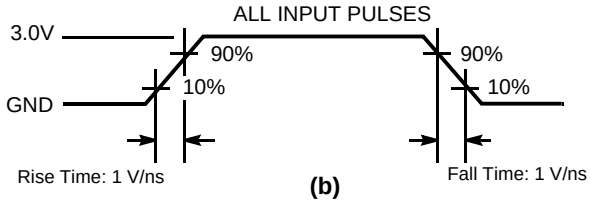
2. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

[+] Feedback

AC Test Loads and Waveforms[4]

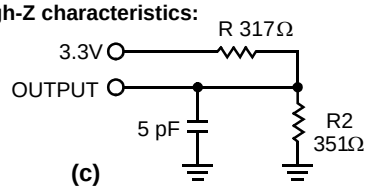


(a)



(b)

High-Z characteristics:



(c)

Switching Characteristics Over the Operating Range[5]

Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		5		6		7	ns
t_{PU}[8]	$\overline{CE}$ LOW to Power-up	0		0		0		ns
t_{PD}[8]	$\overline{CE}$ HIGH to Power-down		10		12		15	ns
Write Cycle[9, 10]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		ns
t_{AW}	Address Set-up to Write End	8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Set-up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		5		6		7	ns

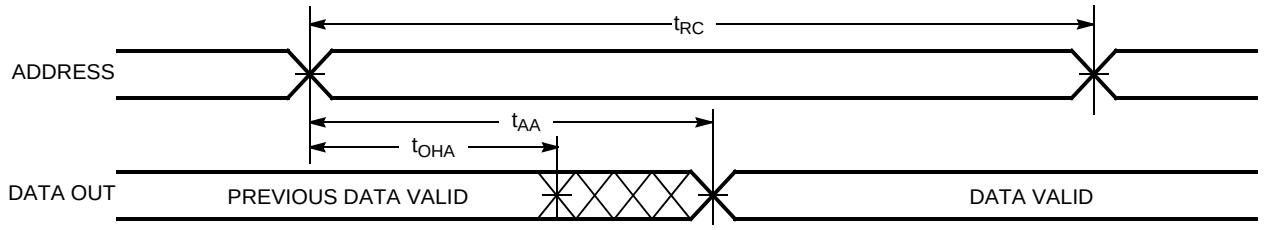
Notes:

4. AC characteristics (except High-Z) for all speeds are tested using the Thèvenin load shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. This parameter is guaranteed by design and is not tested.
9. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

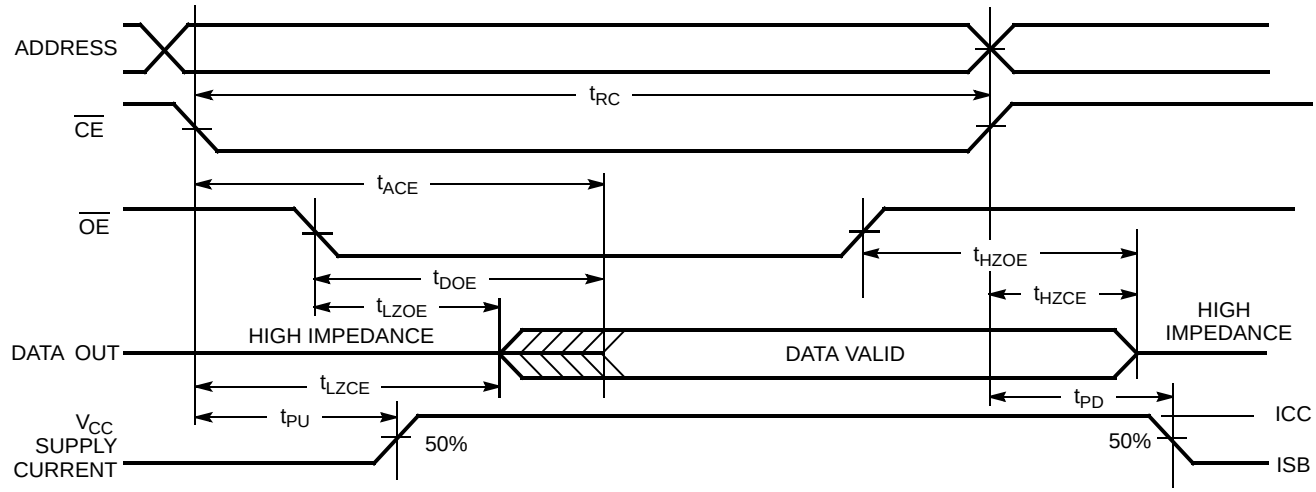
[+] Feedback

Switching Waveforms

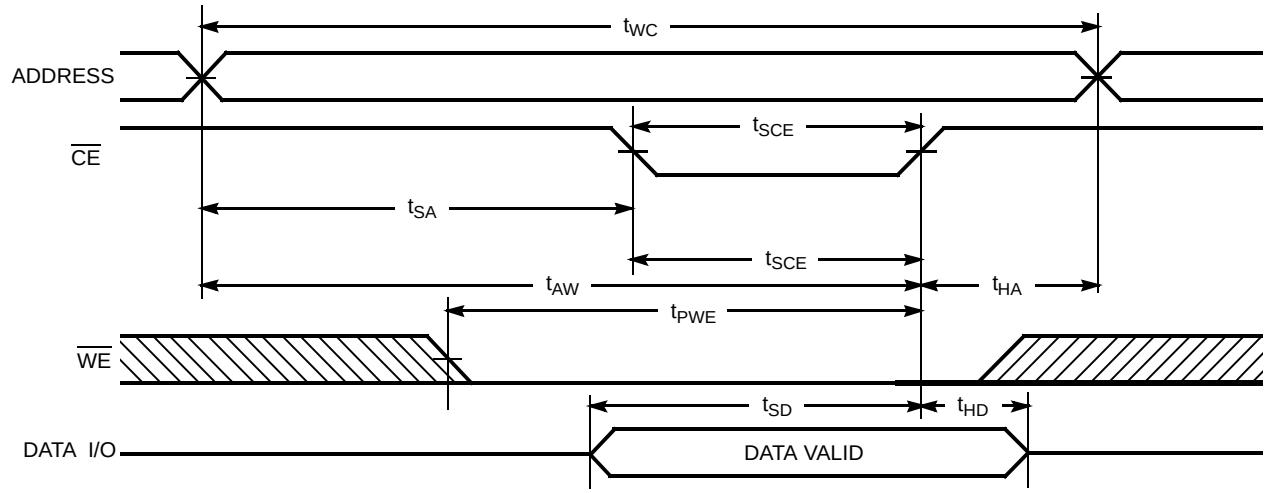
Read Cycle No. 1[11, 12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]



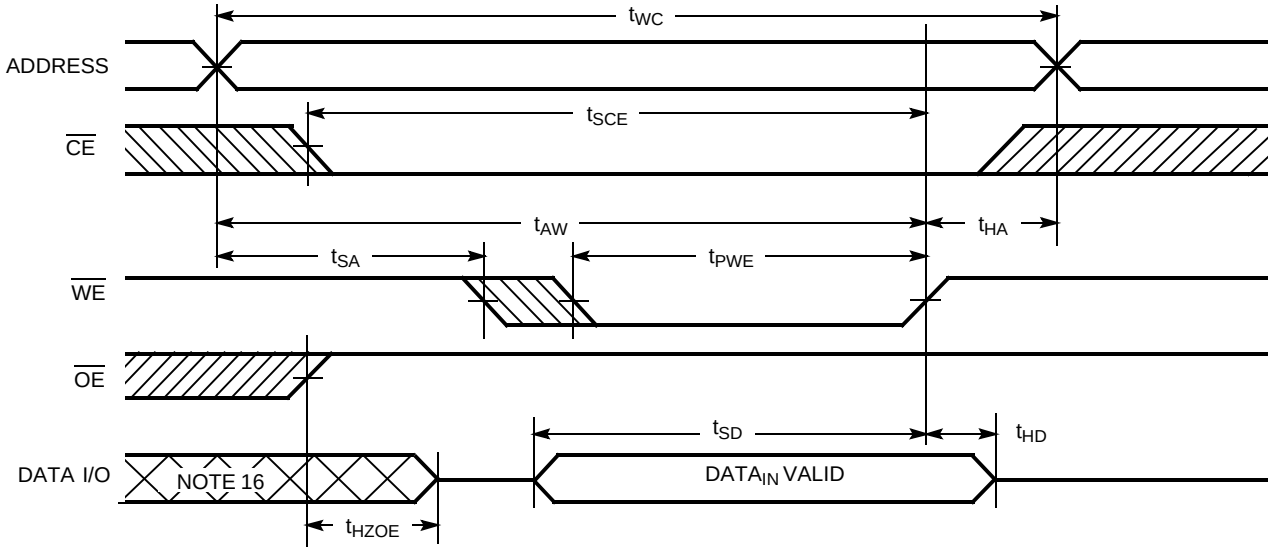
Notes:

11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for Read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

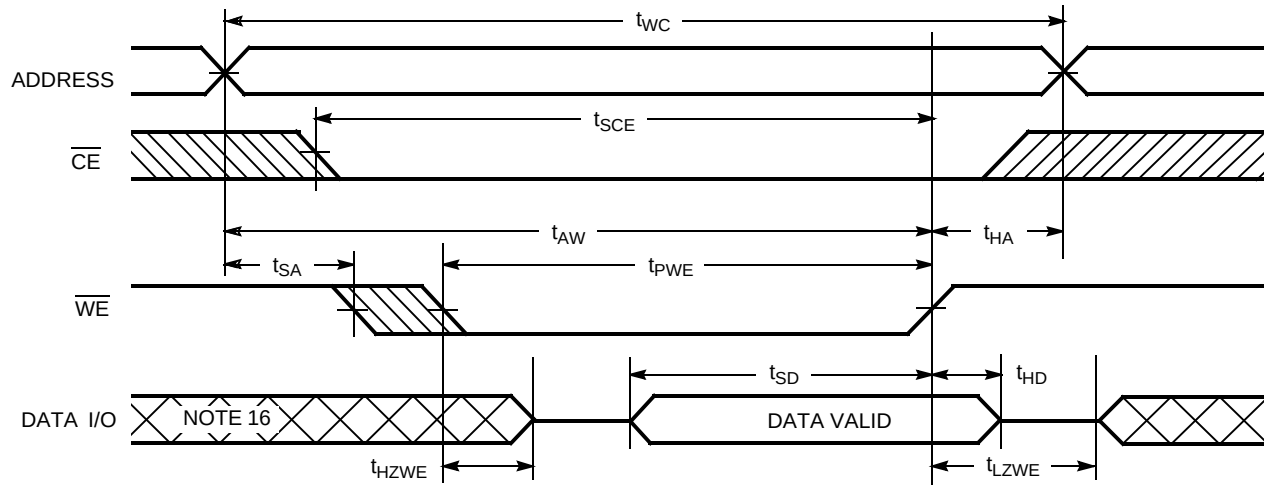
[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14, 15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 15]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Note:
16. During this period the I/Os are in the output state and input signals should not be applied.

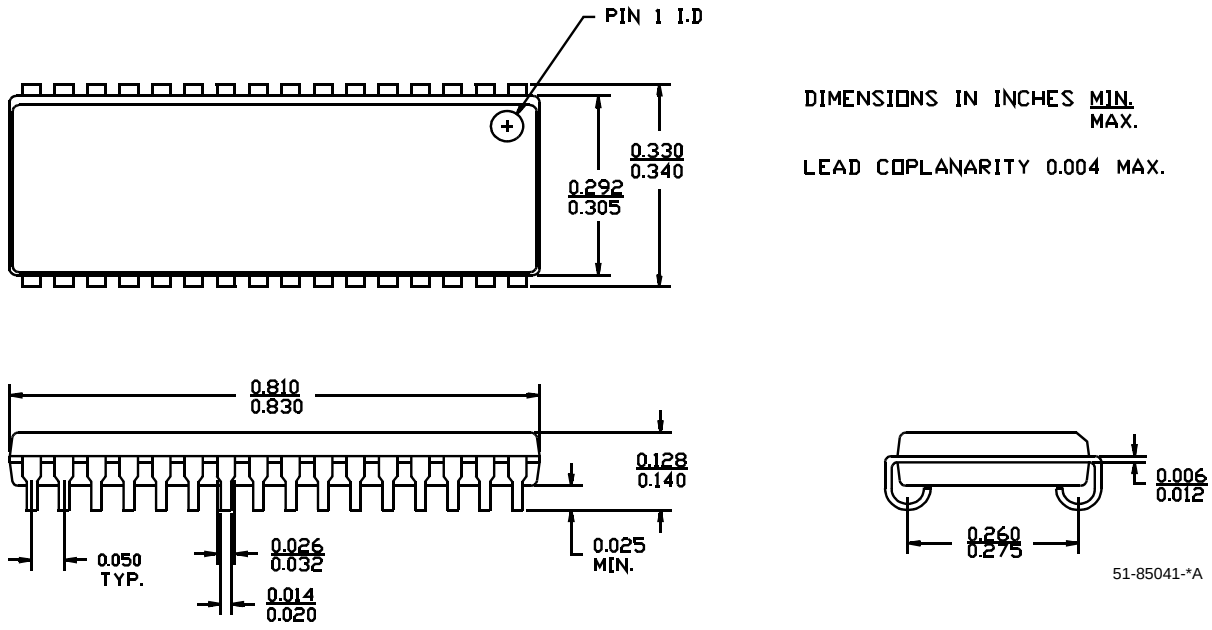
[+] Feedback

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1018CV33-10VC	51-85041	32-lead 300-mil Molded SOJ	Commercial
12	CY7C1018CV33-12VC		32-lead 300-mil Molded SOJ	Commercial
	CY7C1018CV33-12VXI		32-lead 300-mil Molded SOJ (Pb-Free)	Industrial
15	CY7C1018CV33-15VXC		32-lead 300-mil Molded SOJ (Pb-Free)	Commercial

Package Diagram

32-lead (300-mil) Molded SOJ (51-85041)



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Document History Page

Document Title: CY7C1018CV33 128K x 8 Static RAM Document Number: 38-05131				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109426	12/14/01	HGK	New Data Sheet
*A	113432	04/10/02	NSL	AC Test Loads split based on speed
*B	115046	05/30/02	HGK	I_{CC} and I_{SB1} modified
*C	116476	09/16/02	CEA	Add applications foot note on data sheet, pg 1
*D	493543	See ECN	NXR	Added Industrial Operating Range Removed 8 ns speed bin from Product offering Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated the Ordering Information Table

[+] Feedback